Confirmation No. 9022 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	VAN HOUDT *et al.*	Examiner:	Perilla, J.
Serial No.:	10/538,576	Group Art Unit:	2611
Filed:	June 15, 2005	Docket No.:	NL021302US1 (NXPS.520PA)
Title:	FRAME SYNCHRONIZING DEVICE AND METHOD		

APPEAL BRIEF

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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed July 13, 2009 and in response to the rejections of claims 1-15 as set forth in the Final Office Action dated August 22, 2008.

Please charge Deposit Account number 50-4019 (NL021302US1) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-15 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated August 22, 2008.

V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a frame synchronizing device for a binary data transmission system wherein digital data are transmitted as a serial bit stream organized into frames, each frame

including a pre-defined frameheader (*see, e.g.,* page 1:1-12 and page 6:23 to page 7:17), the device comprising: a serial input parallel output shift register for receiving said serial bit stream and outputting said frames in a consecutive order, said shift register including a serial input portion and a parallel output portion and having at least as many stages as the number of bits of a frame (*see, e.g.,* serial and parallel shift registers shown in Fig. 4), first clock circuitry that generates first clock pulses, separated by a first time period, for clocking the serial input portion of the shift register (*see, e.g.,* serial clock shown in Fig. 4); second clock circuitry that generates second clock pulses for clocking the parallel output portion of the shift register, the second clock circuitry generating the second clock pulses responsive to the first clock pulses (*see, e.g.,* clock divided by N counter shown in Fig. 4), and control circuitry for detecting whether or not a frameheader is present at the output of said parallel output portion and, if not, controlling said shift register so that the clocking of the parallel output portion is delayed by at least the first time period, the control circuitry delaying the clocking of the parallel output portion by preventing one of the first clock pulses from reaching the second clock circuitry (*see, e.g.,* Fig. 5 and page 7:20-33).

Commensurate with independent claim 8, an example embodiment of the present invention is directed to a frame synchronizing method for a binary data transmission system wherein digital data are transmitted as a serial bit stream organized into frames, each frame including a pre-defined frameheader (*see, e.g.,* page 1:1-12 and page 6:23 to page 7:17), the method comprising the steps of: inputting said serial bit stream (*see, e.g.,* serial data shown in Fig. 4) into a serial input portion of a serial input parallel output shift register having at least as many stages as the number of bits of a frame (*see, e.g.,* serial and parallel shift registers shown in Fig. 4), generating first clock pulses, by first clock circuitry, for clocking the serial portion of the shift registers, the first clock pluses separated by a first time period (*see, e.g.,* serial clock shown in Fig. 4), generating second clock pulses, by second clock circuitry, for clocking a parallel output portion of the shift register, the second clock pulses derived from the first clock pulses (*see, e.g.,* clock divided by N counter shown in Fig. 4), outputting said frames in a consecutive order from the parallel output portion of said shift register (*see, e.g.,* page 1:10-12), detecting whether or not a frameheader is present in the output of said parallel output portion, and, if not, delaying the generation of the second clock

pulses by at least the first time period by preventing one of the first clock pulses from reaching the second clock circuitry (*see, e.g.,* Fig. 5 and page 7:20-33).

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1-14 stand rejected under 35 U.S.C. §102(b) over Buckland (U.S. Patent No. 4,744,081).

B. Claim 15 stands rejected under 35 U.S.C. §103(a) over Buckland (U.S. Patent No. 4,744,081) in view of Giorgetta (U.S. Patent No. 7,035,292).

VII. Argument

The rejections of claims 1-15 cannot be maintained because the '081 reference does not correspond to the claimed invention as asserted and because the rejections rely upon a blatant mischaracterization of the teachings of the '081 reference. In fact, the '081 reference is largely cumulative of prior art disclosed in Appellant's specification (*e.g.,* U.S. Patent No. 4,675,886), which involves providing a signal to a divider to change the number by which a clock signal is divided (*e.g.,* signal SLIP that is provided to divider 20 in the '081 reference). The Examiner mischaracterizes these cumulative teachings of the '081 reference by taking a single paragraph out of context and improperly alleging correspondence to the claimed invention.

Appellant's claimed invention delays the clocking of a parallel output portion of a shift register by holding an output clock for one high frequency clock cycle (*e.g.,* "preventing one of the first clock pulses from reaching the second clock circuitry"), thereby synchronizing a counter (*e.g.,* a divider) to the serial bitsteam using low frequency driving signals. Such an approach allows for improved efficiency of the frame synchronization and lower power dissipation. The '081 reference, however, does not prevent any clock pulses from reaching divider 20 and the '081 reference does divide the serial clock signal in the presence of the signal SLIP, in contrast to the Examiner's erroneous assertions.

A. The § 102(b) Rejection Is Improper Because The '081 Reference Does Not Disclose Preventing First Clock Pulses From Reaching Second Clock Circuitry

The '081 reference does not teach delaying the clocking of a parallel output portion by preventing one of the first clock pulses from reaching the second clock circuitry, as in the claimed invention. The Examiner's assertion that control circuit 10 somehow prevents clock pulses on line 26 (*i.e.*, the asserted first clock pulses) from reaching divider 20 (*i.e.*, the asserted second clock circuitry) is directly contradicted by the '081 reference. In fact, the '081 reference clearly teaches that each and every clock pulse of the serial clock on line 26 is provided to the divider 20. *See, e.g.*, Figure 1, reproduced below for the convenience of the Board. The signal SLIP provided by control circuit 10 simply instructs the divider 20 to change the number by which it divides the serial clock for one division cycle. *See, e.g.*, Col. 2:61-65 and Col. 3:28-33. Therefore, the control circuit 10 cannot possibly prevent one of the clock pulses on line 26 from reaching the divider 20.

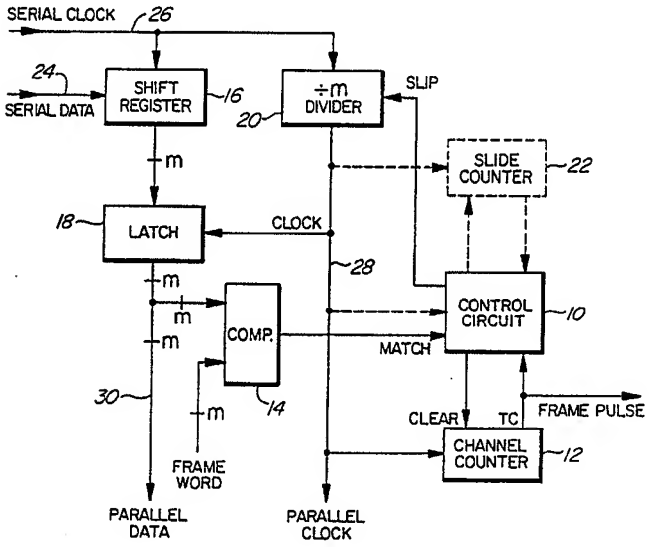

FIG. 1

In the Advisory Action, the Examiner continues to mischaracterize the teachings of the '081 reference in asserting that the '081 reference teaches that the divider 20 "only performs" dividing of the serial clock signal in the absence of the signal SLIP provided by control circuit 10. The Examiner's assertion is directly contradicted by the '081 reference and is but a failed attempt to maintain the rejection despite the clear lack of correspondence to the claimed invention. In fact, the divider 20 still divides the serial clock signal in the presence of the signal

SLIP, which merely causes the divider 20 to change the number by which the serial clock signal is divided (*e.g.*, divide by m in the absence of the signal SLIP and divide by m-l or m+1 when the signal SLIP is provided). *See, e.g.,* Col. 2:61-65 and Col. 3:28-33. For example, the '081 reference states that "control circuit 10 supplies the signal SLIP to the divider 20 to cause the divider to slip by on pulse of the serial clock on the line 26; i.e. to divide by m-1 or m+1 for one division cycle." As such, the signal SLIP does not prevent any clock pulses of the serial clock signal from reaching the divider 20, but instead instructs the divider to change the number by which it divides the serial clock signal. In other words, the divider 20 still receives each and every one of the clock pulses of the serial clock signal, with the signal SLIP simply instructing the divider 20 to change the number of clock pulses of the serial clock signal that are counted by the divider 20 before it outputs a clock signal on line 28.

In view of the above, the '081 reference does not correspond to the claimed invention. In particular, the Examiner's blatant mischaracterization of the teachings of the '081 reference is directly contradicted by the '081 reference and, as such, does not support the Examiner's position that the '081 reference teaches preventing clock pulses from reaching divider 20. Instead, the '081 reference expressly teaches that each and every one of the clock pulses of the serial clock signal are counted by the divider 20, as discussed above. Accordingly, Appellant respectfully submits that the § 102(b) rejection is improper and requests that it be withdrawn.

B. The § 103(a) Rejection Is Improper Because The '081 Reference Does Not Correspond To The Claimed Invention And Because The Asserted Basis To Combine Is Contrary To The Requirements Of § 103 And Relevant Law

As discussed above, the '081 reference does not correspond to the claimed invention. Appellant submits that the '292 reference does not address the above discussed deficiencies of the '081 reference. For example, neither reference teaches delaying the clocking of a parallel output portion by preventing one of the first clock pulses from reaching the second clock circuitry. Because neither reference teaches these aspects, no reasonable combination of these references can provide correspondence to the claimed invention. As such, in the context of *KSR*, the asserted combination "as a whole" is entirely unpredictable based on the asserted teachings of the cited references.

Moreover, the Examiner fails to provide a valid reason for the proposed combination of the asserted references. "A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art." *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007) ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art."). In this instance, the Examiner asserts that it would be obvious to the skilled artisan that the device of the '081 reference could be applied as a frame synchronization device in a SONET or Gigabit Ethernet application because "such applications require frame synchronization and are well known in the art." As such, the Examiner merely asserts that such aspects are well known, without providing any reason why the skilled artisan would modify the '081 reference. The recent Supreme Court decision supports the long-standing law that the mere existence of elements in the prior art is not sufficient for a § 103 rejection:

> Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007).

Thus, it is not sufficient to simply assert that such aspects are well-known. The Examiner must also provide a reason why the skilled artisan would modify the '081reference in order to maintain the § 103 rejection.

In view of the above, Appellant respectfully submits that the § 103(a) rejection is improper and requests that it be withdrawn.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-15 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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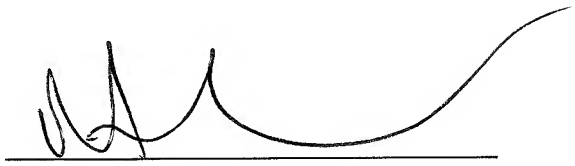
By: 

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/538,576)

1. A frame synchronizing device for a binary data transmission system wherein digital data are transmitted as a serial bit stream organized into frames, each frame including a pre-defined frameheader, the device comprising:

a serial input parallel output shift register for receiving said serial bit stream and outputting said frames in a consecutive order, said shift register including a serial input portion and a parallel output portion and having at least as many stages as the number of bits of a frame,

first clock circuitry that generates first clock pulses, separated by a first time period, for clocking the serial input portion of the shift register;

second clock circuitry that generates second clock pulses for clocking the parallel output portion of the shift register, the second clock circuitry generating the second clock pulses responsive to the first clock pulses, and

control circuitry for detecting whether or not a frameheader is present at the output of said parallel output portion and, if not, controlling said shift register so that the clocking of the parallel output portion is delayed by at least the first time period, the control circuitry delaying the clocking of the parallel output portion by preventing one of the first clock pulses from reaching the second clock circuitry.

2. The device according to claim 1, wherein said control circuitry is adapted so that the preventing of one of the first clock pulses from reaching the second clock circuitry is repeated until synchronization is reached.

3. The device according to claim 1, wherein the frames have a fixed length.

4. The device according to claim 3, wherein the frames are bytes.

5. The device according to claim 1, wherein the control circuitry is adapted to control

said second clock circuitry so that said second clock pulses are delayed by at least the first time period which is needed for shifting a bit in said serial input portion from a stage to a next stage.

6. The device according to claim 5, wherein each frame includes N bits, and the second clock circuitry converts said first clock pulses into said second clock pulses, the second clock pulses separated by a second time period that is N times longer than the first time period of said first clock pulses, said control circuitry is adapted to control said second clock circuitry so that said second clock pulses are delayed by at least the first time period of said first clock pulses.

7. The device according to claim 5, wherein said control circuitry is adapted to supply a control signal to said second clock circuitry to prevent the one of the first clock pulses from reaching the second clock circuitry, and said second clock circuitry is adapted so that the one of the first clock pulses is blocked by said control signal for at least the first time period which is needed for shifting a bit in said serial input portion of said shift register from a stage to a next stage.

8. A frame synchronizing method for a binary data transmission system wherein digital data are transmitted as a serial bit stream organized into frames, each frame including a pre-defined frameheader, the method comprising the steps of:

inputting said serial bit stream into a serial input portion of a serial input parallel output shift register having at least as many stages as the number of bits of a frame,

generating first clock pulses, by first clock circuitry, for clocking the serial portion of the shift registers, the first clock pluses separated by a first time period

generating second clock pulses, by second clock circuitry, for clocking a parallel output portion of the shift register, the second clock pulses derived from the first clock pulses,

outputting said frames in a consecutive order from the parallel output portion of said shift register,

detecting whether or not a frameheader is present in the output of said parallel output portion, and,

if not, delaying the generation of the second clock pulses by at least the first time period by preventing one of the first clock pulses from reaching the second clock circuitry.

9. The method according to claim 8, wherein the preventing of one of the first clock pulses from reaching the second clock circuitry is repeated several times until synchronization is reached.

10. The method according to claim 8, wherein the frames have a fixed length.

11. The method according to claim 10, wherein the frames are bytes.

12. The method according to claim 8, the second clock pulses are delayed by at least the first time period which is needed for shifting a bit in said serial input portion from a stage to a next stage.

13. The method according to claim 12, comprising the further steps of:

converting said first clock pulses into said second clock pulses, the second clock pulses separated by a second time period that is N times longer than the first time period of said first clock pulses, wherein each frame includes N bits, and said second clock pulses are delayed by at least the first time period of said first clock pulses.

14. The method according to claim 12, further comprising generating a control signal if a frameheader is not detected in the output of said parallel output portion of said shift register, and blocking the generation of said second clock pulses by said control signal for at least the first time period which is needed for shifting a bit in said serial input portion of said shift register from a stage to a next stage.

15. A digital data transmission systems like SONET/SDH or Gigabit Ethernet comprising a device as claimed in claim 1 where serial data are transported over a single channel and, at the receiving side, is converted into parallel data for further processing.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.